**Lab 9: Finite State Machine Analysis**

Freddie Boadu

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Mansi Bhavsar

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**Introduction:**

This lab was about teaching students how to make a finite state machine. A finite state machine allows the machine to go from state to state and be cleared. It can also go to a previous state.

**Materials:**

* Xilinx ISE software, student or professional edition V14.7
* Digilent Basys2 board with an XC3S100E device.

**Methods:**

The student was asked to make a new project. The student called the project Lab 9. The student is asked to complete the same circuit on the lab. That circuit will be provided in the data section. The student is then asked to figure out and test all the states and their outputs.

**Data:**

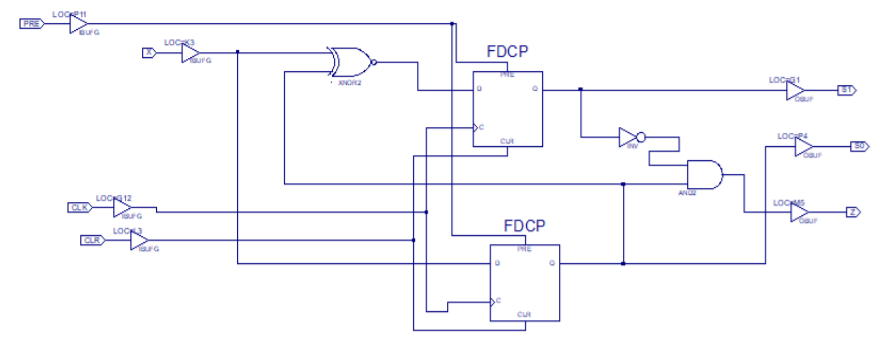
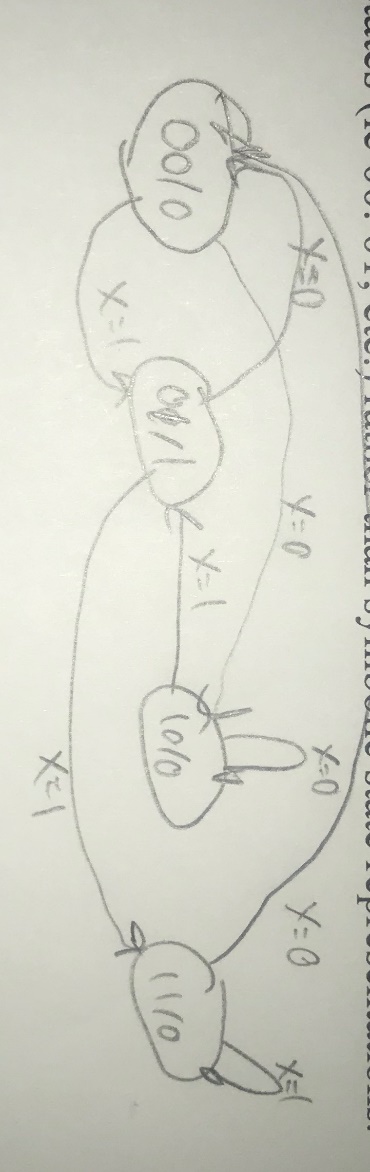


Figure 1: Finite state machine schematic

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| X | S1 | S0 | D1 | D0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Present State | | | | Next state | | | Z |
|  |  | X=0 | | | X=1 | |  |
| S1 | S0 | S0’ | S1’ | | S1’ | S0’ |  |
| 0 | 0 | 1 | 0 | | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | | 1 | 1 | 0 |



**Results and Discussion:**

The schematic proved to be true. As the student tested the machine all the states were correct and came out to the results started on the truth table in data. There was no design challenge for this lab.

**Conclusion:**

In this lab the student learned to understand how a finite state machine works. As the student learned how the state machine worked, the student learned to test all the possible outputs of the machine to make sure all the states are reached.